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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/911,851	07/25/2001	Hak Su Kim	CIT/K-152	3915

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EXAMINER	
LESPERANCE, JEAN E	

ART UNIT	PAPER NUMBER
2674	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/911,851	KIM, HAK SU
	Examiner	Art Unit
	Jean E Lesperance	2674

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims and 21-29

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29* is/are allowed.

6)☒ Claim(s) *1-3,6,21-23,25,27 and 28* is/are rejected.

7)☒ Claim(s) *4,5,24 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Claims 1-6 and 21-29 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 6, 21-23, 25, 27, and 28 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent # 5,532,712 ("Tsuda et al.") in view of US Patent # 6,598,148 ("Moore et al.).

As for claim 1, Tsuda et al. teach a Vcc connected to the shift register acting as a power supply (Fig.8) corresponding to a DC-DC converter provided inside one chip, for controlling an external voltage input depending on a timing control signal and providing a controlled DC voltage; the PC terminal is connected through an inverter 3c to a first input of each of the plurality of gate circuits 2b (column 6, lines 64-66) corresponding to an interface unit provided inside the chip, for interface with parts outside the chip; shift register Fig.8 (3a) corresponding to a memory provided inside the chip, for storing

display information transmitted through the interface unit: latch Fig.8 (3b) corresponding to a data processor provided inside the chip, for providing a display data to a display panel of the EL display device using the display information stored in the memory and the controlled DC voltage output from the DC-Dc converter; a plurality of first gate circuits 2a and a plurality of second gate circuits 2b (Fig.8) corresponding to a scan processor provided inside the chip, for outputting scan data to the display panel using the display information and the controlled DC-voltage output from the DC-DC converter: and the clock terminal connected to the latch 6b and through an inverter 3e to the shift register 3a (column 7, lines 38-39) corresponding to a timing control unit provided inside the chip, for providing the timing control signal to the DC-DC converter, the interface unit, the memory, the data processor, and the scan processor. Accordingly, the prior art does teach all the claimed limitations as recited in claim 1 with the exception of providing a DC-DC converter inside the chip.

However, Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip and The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly (Fig.2) where the DC-DC converter is converting external voltage which is the output voltage uses to shift register to drive the CRT display.

Thus, it would have been obvious to a person of ordinary skill in the art to utilize the DC-DC converter as taught by Moore et al. in the drive circuit disclosed by Tsuda et

al. because this would have provide a high performance IC that can be connected to DRAM without sacrificing the IC speed.

As for claim 2, Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip which is connected to the power peripheral outside corresponding to power peripheral unit provided outside the chip, for controlling input and output voltages of the DC-DC converter, preventing a backward current from occurring during the DC-DC conversion, and maintaining the input DC voltage for a predetermined-time.

As for claim 3, Moore et al. teach an DC-DC converter Fig.7 (294) and it is inherent to any power peripheral to include inductor, diode, and resistor.

As for claim 6, Tsuda et al. teaches an insulated converter DC-DC converter 11 and it is outside the device 3 where it inherent that impedance generating unit and resistor can be installed outside device 3.

As for claims 21 and 22, Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip that controls the external voltage and it is inherently depends on timing control signal because everything is timing inside the chip.

As for claims 23, 27, and 28, Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip and The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly (Fig.2) where the DC-DC converter is converting external voltage which is the output voltage uses to shift register to drive the CRT display which a load condition of a feedback signal.

As for claim 25, Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip and The microprocessor 50 has a DMA capability which can be used for I/O to a video shift register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly (Fig.2) where the DC-DC converter is converting external voltage which is the output voltage uses to shift register to drive the CRT display where inherently there a timing to control the feedback between input and output.

Allowable Subject Matter

Claims 4, 5, 24, and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 29 is allowed.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

The following is a statement of reasons for the indication of allowable subject matter: the claimed invention is directed to a driving circuit for a display device. Dependent claims 4 identifies a uniquely distinct feature "a first capacitor connected with the input terminal in parallel to minimize fluctuation of the input voltage; a second capacitor connected with the output terminal in parallel to minimize fluctuation of the controlled DC voltage; an inductor connected in series between the input terminal and

the output terminal, for maintaining the external voltage applied to the DC-DC converter for a predetermined time; and a diode connected in series between the input terminal and the output terminal, for preventing a backward current from occurring". Dependent claim 5 identifies a uniquely distinct feature "a resistor connected with an output terminal of a DC-DC converter in parallel and with an output terminal of the impedance generating unit in series; and a voltage control unit receiving a feedback value of the controlled Dc voltage distributed by the impedance value output from the impedance generating unit and a value of the resistor, and then outputting a DC voltage controlled according to the feedback voltage". Dependent claim 24 identifies a uniquely distinct feature "a voltage control unit having an input terminal that receives the external voltage, an output terminal and a feedback terminal; and a feedback circuit coupled between the output terminal and the feedback terminal that controls the feedback signal according to the timing control signal". Dependent claim 26 identifies a uniquely distinct feature "a voltage control unit having an input terminal that receives the external voltage, an output terminal and a feedback terminal; and a mode control unit that receives the timing control signal, wherein the control DC voltage can be generated by the DC-DC converter for a plurality of modes according to a feedback signal received at the feedback terminal that corresponds to a voltage control signal output by the mode control signal". Independent claim 29 identifies a uniquely distinct feature "resistance means coupled to an output terminal of the DC-DC converter for distributing the controlled DC voltage, and voltage control means for receiving a feedback voltage of the controlled Dc voltage distributed by the resistance means responsive to the voltage

control signal of the mode control means, and then outputting the Dc voltage controlled according to the feedback voltage".

The closest arts, Tamanoi and Tsuda et al. and Moore et al. as discussed above, either singularly or in combination, fail to anticipate or render the above limitations obvious.

Response to Amendment

Applicant's arguments filed 4-28-2004 have been fully considered but they are not persuasive. The applicant argued that the previous restriction does contain serious burden on the examiner to examiner all the claims 1-20. Examiner disagrees with the applicant because Restriction to one of the following inventions is required under 35 U.S.C. 121: Group I. Claims 1-6 and 8-20, drawn to a display driving control circuit, classified in class 345, subclass 204.Group II. Claim 7, drawn to a reactive power control, classified in class 323, subclass 205. The inventions are distinct, each from the other because: Group I which is a display driving control circuit is functional on its own and does not need Group I. Group II which is a reactive power control can function independently from Group I. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper. The applicant argued that the prior art does not a driving circuit for a display device including a DC-DC converter provided inside the chip. Examiner disagrees with the applicant because Moore et al. teach a DC-DC converter Fig.7 (294) inside the chip and The microprocessor 50 has a DMA capability which can be used for I/O to a video shift

register. The microprocessor 310 uses yet another 1024-bit column latch as a long video shift register to drive a CRT display directly (Fig.2) where the DC-DC converter is converting external voltage which is the output voltage uses to shift register to drive the CRT display which a load condition of a feedback signal. Therefore the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean Lesperance whose telephone number is (703) 308-6413. The examiner can normally be reached on from Monday to Friday between 8:OOAM and 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Richard Hjerpe, can be reached on (703) 305-4709 .

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Jean Lesperance

Art Unit 2674

Date 6-29-2004

XIAO WU
PRIMARY EXAMINER